UNITED STATES PATENT AND TRADEMARK OFFICE

A

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/932,891	08/20/2001	Jens Sauerbrey	L&L-10050	6815

24131 7590 10/20/2005

LERNER AND GREENBERG, PA
P O BOX 2480
HOLLYWOOD, FL 33022-2480

EXAMINER	
CHEN, TSE W	
ART UNIT	**PAPER NUMBER**
2116	

DATE MAILED: 10/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/932,891	SAUERBREY ET AL.	
	Examiner	Art Unit	
	Tse Chen	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 7-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 7-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

In view of the Appeal Brief filed on July 25, 2005, PROSECUTION IS HEREBY REOPENED. New grounds of rejection are set forth below.

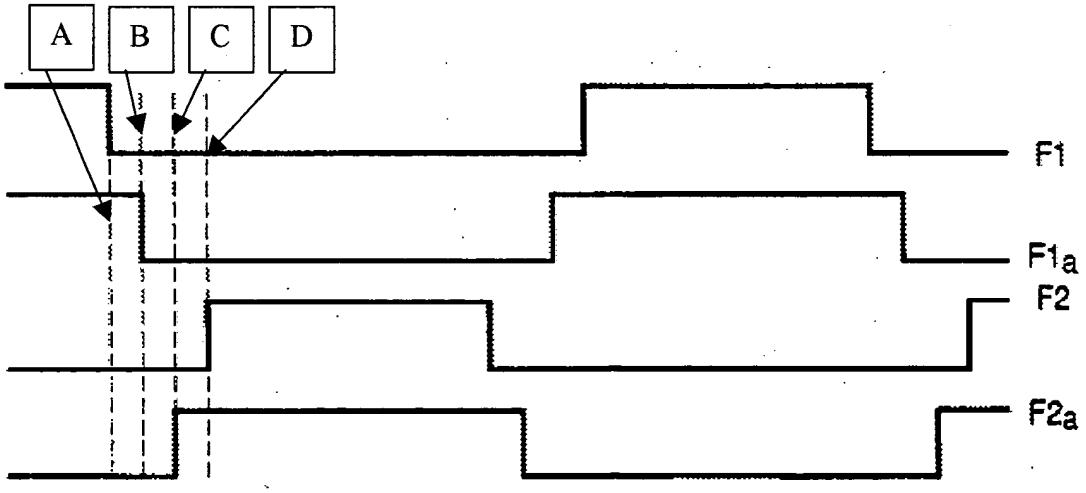
To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31. A new notice of appeal fee and appeal brief fee will not be required for applicant to appeal from the new Office action. Any appeal brief filed on or after September 13, 2004 must comply with 37 CFR 41.37.

Findings

5. Baschirotto et al., U.S. Patent 5745002, hereinafter Baschirotto, discloses:



5.1. A circuit configuration in switched op-amp technology [fig.9; col.4, ll.21-23].

5.2. The circuit configuration comprising at least one switchable operational amplifier [A2] having an input [S4] and an output [VO] [fig.4] and transistors having a switching speed [fig.10; inherently, transistors have associated switching speed dependent upon their respected dimensions].

5.3. The circuit configuration comprising at least one sampling capacitor [switched or sampling capacitance C1] connected to said input.

5.4. The circuit configuration comprising at least one integrating capacitor [feedback capacitance C2] connected to said input and to said output.

5.5. The circuit configuration comprising a clock generator [inherently, there is a clock generator, *in the broadest interpretation*, to produce the signals] producing at least two non-overlapping switching-clock signals [fig.5, F1a and F2a].

5.6. Each clock signal having switching-clock phases including an on-phase and an off-phase [col.8, ll.1-8, l.60 – col.9, l.14].

5.7. Said at least two non-overlapping switching-clock signals including a first switching-clock signal [F1a] and a second switching-clock signal [F2a].

5.8. Said clock generator controlling charging of said sampling capacitor with said first switching-clock signal [col.9, ll.7-10] and switching said operational amplifier on and off with said second switching-clock signal [col.9, ll.10-14; controls on/off of output].

5.9. A circuit configuration [fig.8] in fully differential circuit technology [col.4, ll.1-15; the signal lines and voltage settings of the circuit configuration of fig.4 may also be set accordingly to derive the fully differential configuration].

5.10. A method for clocking successive operation amplifier stages [fig.9; op-amp 1, 2, and 3 form successive stages] constructed in switched op-amp technology [col.4, ll.21-23].

5.11. The method comprising generating at least two non-overlapping switching-clock signals [F1a and F2a] [fig.5; col.8, ll.1-8, l.60 – col.9, l.14].

5.12. The method comprising switching a first operational amplifier [A1] on and off with a first signal [F1a] of the two switching-clock signals [col.9, ll.40-44].

5.13. The method comprising switching a second operational amplifier [A2] on and off with a second signal [F2a] of the switching-clock signals [col.9, ll.58-62].

5.14. The method comprising providing a delay between the switching-clock phases of the first [F1a] and second signals [F2a] during which the operational amplifiers are switched off [fig.5; providing of delay conceded by Applicant as noted in previous Office Action].

5.15. The advantage is to reduce the amplitude of negative switching spikes by anticipating the turning on of the input/output switched operational amplifiers and driving the switches with clock phase signals suitably delayed [fig.5; col.7, l.62 – col.8, l.5; myriads of factors well known in the art may influence the turning on of the input/output switched operational amplifiers].

6. Fletcher, U.S. Patent 6392466, discloses:

6.1. A circuit configuration [cache 700; fig.3] in switched amplifier [sense amplifier 620] technology [fig.5; col.3, l.46 – col.4, l.2].

6.2. The circuit configuration comprising a clock generator [703].

6.3. The circuit configuration comprising a phase-variance device [controllable pulse clock delay block 790] varying said switching-clock phases in which the first and second

switching-clock signals are in off-phase and providing a variable delay between the switching-clock phases of the first and second signals [fig.6; col.21, l.19 – col.22, l.5; control signals enable phase two to be off-phase relative to phase one].

6.4. Said phase-variance device connected to said clock generator [fig.3].

6.5. The advantage of utilizing phase variance in circuits is reduction in power consumption [col.8, ll.41-65; col.17, l.33 – col.19, l.11; col.20, l.50 – col.21, l.18; pulse clock delay arrangement utilizing amplifiers varies phase and thus, produces a pulse with suitable width to save processing time which saves power].

7. Saito et al., U.S. Patent 5723998, hereinafter Saito, discloses:

7.1. A circuit configuration, comprising a detector [operating speed measurement 121] for detecting the switching speed of the transistors, the detector being connected to an operational amplifier [comparator 139] [col.5, l.35 – col.6, l.39].

7.2. The advantage of utilizing a transistor speed detector is optimization of processing according to operating condition [col.1, ll.49-67].

8. Varadarajan, U.S. Patent 4551638, discloses:

8.1. A circuit configuration comprising a device [ECL gate] for enlarging a duration [from activation of driving signal which switches the transistor to onset of delay] when a switching speed is high and reducing the duration when the switching speed is low [switching speed is inversely related to delay] [col.3, ll.42-57].

8.2. The advantage of enlarging a duration when a switching speed is high and reducing the duration when the switching speed is low is to reduce power consumption without adversely affecting performance.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 17-21 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baschirotto in view of Fletcher.

11. In re claim 17, Baschirotto discloses each and every limitation as set forth in findings 5.10-5.14. Baschirotto discloses that the amplitude of negative switching spikes can be reduced by anticipating the turning on of the input/output switched operational amplifiers and driving the switches with clock phase signals suitably delayed [finding 5.15], without explicitly declaring the utilization of a well known phase variance device, which one with ordinary skill in the art would recognize as being suitable for use in providing the suitably delayed clock phase signals in a convenient fashion [i.e., without having to reinstall a new clock generator every time one of a myriad of factors affecting the turning on of the input/output switched operational amplifiers changes].

12. Fletcher explicitly discloses the phase variance device [finding 6.3] suitable for use with the switched operational amplifier system of Baschirotto [both utilize transistor amplifiers].

13. It would have been obvious to one of ordinary skill in the art, having the teachings of Baschirotto and Fletcher before him at the time the invention was made, to use the phase-variance device taught by Fletcher with the switched operational amplifier system disclosed by Baschirotto as the well known phase-variance device explicitly taught by Fletcher is

suitable for use in providing the suitably delayed clock phase signals in a convenient fashion to reduce the amplitude of negative switching spikes [finding 5.15]. One of ordinary skill in the art would have been motivated to make such a combination as it provides a well known way to conveniently provide the suitably delayed clock phase signals necessary to reduce the amplitude of negative switching spikes.

14. As to claim 18, Baschirotto and Fletcher discloses the method comprising varying each of the switching-clock phases in which the operational amplifiers are switched off, as discussed above in reference to claim 17 above.

15. As to claim 19, Fletcher discloses the method comprising varying each second one of the switching-clock phases in which the operational amplifiers [sense amplifiers] are switched off [col.8, ll.41-65; col.17, l.33 – col.19, l.11; col.20, l.50 – col.21, l.18].

16. As to claim 20, Fletcher discloses the method comprising varying a duration [stretching] of the switching-clock phases in which the operational amplifiers are switched off dependent on a transient response of the operational amplifiers [col.8, ll.41-65; col.17, l.33 – col.19, l.11; col.20, l.50 – col.21, l.18; timing requirements depend on transient response of components].

17. As to claim 21, Fletcher discloses the method comprising varying a duration of the switching-clock phases in which the operational amplifiers are switched off dependent on a switching speed of transistors of the operational amplifiers [col.8, ll.41-65; col.17, l.33 – col.19, l.11; col.20, l.50 – col.21, l.18; timing requirements depend on switching speed].

18. As to claim 24, Baschirotto discloses the method comprising adjusting a duration of the switching-clock phases in which the operational amplifiers are switched off in a number of predetermined steps [col.7, l.62 – col.8, l.5; anticipating the switching function to control the

negative spikes suggests a method comprising a number of predetermined steps such as taking in the current relevant values of clock, voltage, etc., comparing the values to some predetermined value, and then act accordingly in order to derive appropriate timing].

19. Claims 1-5, 9-12, 15-16, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baschirotto and Fletcher as applied to claim 17 above, and further in view of Saito and Varadarajan.

20. In re claim 1, Baschirotto and Fletcher disclose each and every limitation as discussed above in reference to claim 17 and in findings 5.1-5.9 and 6.1-6.3. Baschirotto and Fletcher did not disclose explicitly a detector for detecting the switching speed of the transistors and enlarging a duration when a switching speed is high and reducing the duration when the switching speed is low. Saito discloses a circuit configuration, comprising a detector for detecting the switching speed of the transistors, the detector being connected to an operational amplifier [finding 7.1] in order to optimize processing [findings 6.5, 7.2; phase and frequency are related as is well known in the art]. It would have been obvious to one of ordinary skill in the art, having the teachings of Baschirotto, Fletcher and Saito before him at the time the invention was made, to use the detector taught by Saito for the circuit configuration disclosed by Baschirotto and Fletcher as the detector taught by Saito is suitable for use in the circuit configuration of Baschirotto and Fletcher. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to optimize processing. Varadarajan discloses a circuit configuration comprising a device for enlarging a duration when a switching speed is high and reducing the duration when the switching speed is low [finding 8.1] in order to reduce power consumption without adversely affecting

performance [finding 8.2]. It would have been obvious to one of ordinary skill in the art, having the teachings of Baschirotto, Fletcher and Varadarajan before him at the time the invention was made, to use the explicit teachings of Varadarajan for the circuit configuration disclosed by Baschirotto and Fletcher as the explicit teachings of Varadarajan is suitable for use with the phase-variance device of Baschirotto and Fletcher. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to reduce power consumption without adversely affecting performance.

21. As to claim 2, see discussion above in reference to claim 18.

22. As to claim 3, see discussion above in reference to claim 19

23. As to claim 4, see discussion above in reference to claim 20. Examiner has taken Official Notice that operational amplifiers have an associated transient response [operational amplifiers are signal control devices that operate on electrical power and thus, have a time duration for output power levels to stabilize]. Baschirotto discloses a duration of the switching-clock phases in which the first and second switching-clock signals are in the off-phase dependent upon the transient response of the operational amplifier [col.7, l.62 – col.8, l.5; anticipating the switching function to control the negative spikes suggests utilization of knowledge of transient response in order to derive appropriate timing].

24. As to claim 5, see discussion above in reference to claim 4. Baschirotto discloses the circuit configuration wherein the operational amplifier has transistors [fig.10] having a switching speed [inherently, transistors have associated switching speeds dependent upon their respected dimensions].

25. As to claim 9, Saito discloses the circuit configuration wherein the detector generates detector pulses having a duration characterizing the switching speed of the transistors [col.5, l.35 – col.6, l.38; variable number of pulses of variable duration based on the switching speed of the transistors occupy a predetermined time period to constitute the count value].

26. As to claim 10, Fletcher and Saito disclose the circuit configuration wherein the phase-variance device is configured to adjust a duration of the switching-clock phases in which the first and second switching-clock signals are in the off-phase dependent upon a duration of the detector pulses [see discussion above in reference to claims 1 and 9; detector pulse with variable duration of Saito combined with phase variance device of Fletcher results in adjusting the duration of switching-clock phases in the broadest interpretation].

27. As to claim 11, Fletcher discloses the circuit configuration wherein the phase-variance device is configured to adjust a duration of the switching-clock phases in which the first and second switching-clock signals are in the off-phase in a given number of predetermined steps [col.8, ll.41-65; col.17, l.33 – col.19, l.11; col.20, l.50 – col.21, l.18; e.g., taking in the current relevant values of clock, voltage, etc., comparing the values to some predetermined value, and then act accordingly in order to derive appropriate timing].

28. As to claim 12, Fletcher discloses the circuit configuration wherein the clock generator and the phase-variance device are embodied as a programmable clock generator [col.22, ll.6-35; clock generator and phase-variance device may be integrated as a programmable clock generator for each logical unit].

29. As to claim 15, see finding 5.10 and discussion above in reference to claim 1.

30. As to claim 16, see discussion above in reference to claim 1. In regards to "a means for generating at least two non-overlapping switching-clock signals each having an on-phase and an off-phase", see finding 5.5 where the clock generator represents the means. In regards to "a means for varying switching-clock phases in which said first and second switching-clock signals are in said off-phase", see finding 6.3 where the phase-variance device represents the means.

31. As to claim 28, see discussion above in reference to claims 1 and 17.

32. Claims 7, 30-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baschirotto, Fletcher, Saito and Varadarajan as applied to claims 1, 15-16 above, and further in view of Inoshita et al., US Patent 6477115, hereinafter Inoshita.

33. Baschirotto discloses the circuit configuration wherein the transistors include at least one of n-channel FETs and p-channel FETs [fig.10] and the transistors each have a respective switching speed [inherently, each transistor will have a switching speed in the broadest interpretation]. Saito discloses the detector detects the switching speed of the transistors [col.5, ll.35-57; detector detects switching speed of at least one of the kind of transistors]. Baschirotto and Saito did not disclose explicitly *separately* detecting the switching speed of the n-channel FETs and p-channel FETs.

34. Inoshita discloses a detector separately detecting the switching speed of the n-channel transistors and p-channel transistors [col.9, ll.27-37].

35. It would have been obvious to one of ordinary skill in the art, having the teachings of Inoshita, Baschirotto, Fletcher, Saito and Varadarajan before him at the time the invention was made, to incorporate the teachings of Inoshita with the switched operational amplifier

system disclosed by Baschirotto, Fletcher, Saito and Varadarajan as the well known concept of separately detecting switching speeds of different transistors explicitly taught by Inoshita is suitable for use with the various kinds of circuits that utilizes transistors. One of ordinary skill in the art would have been motivated to make such a combination as it provides a well known way to evaluate characteristics in greater precision and detail [Inoshita: col.9, ll.27-37; separate evaluation provides greater precision for control teachings of Fletcher and Saito].

36. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Baschirotto, Fletcher, Saito and Varadarajan as applied to claim 1 above, and further in view of Chiang, U.S. Patent 5097208.

37. Baschirotto, Fletcher, Saito and Varadarajan disclose each and every limitation of the claim as discussed above in reference to claim 1. In particular, Saito discloses the circuit configuration including an inverter chain [fig.6; inverters 31-35]. Saito did not further discuss the details of the detector.

38. Chiang discloses a detector [testing apparatus 10] [col.1, ll.8-13; delays are related to speed] having an XOR gate [14] with XOR inputs, one of the XOR inputs receiving an undelayed edge signal [B], and another of the XOR inputs receiving the edge signal delayed through the inverter chain [C] [fig.1; col.3, ll.15-34].

39. It would have been obvious to one of ordinary skill in the art, having the teachings of Chiang, Baschirotto, Fletcher, Saito and Varadarajan before him at the time the invention was made, to use the detector taught by Chiang for the circuit configuration disclosed by Baschirotto, Fletcher, Saito and Varadarajan as the detector taught by Chiang is suitable for use in the

circuit configuration of Baschirotto, Fletcher, Saito and Varadarajan. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to determine the speed of an integrated circuit [col.1, ll.8-37; delays are related to speed].

40. Claims 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baschirotto, Fletcher, Saito and Varadarajan as applied to claim 1 above, and further in view of Larson, U.S. Patent 4951303.

41. In re claim 13, Baschirotto, Fletcher, Saito and Varadarajan disclose each and every limitation of the claim, as discussed above in reference to claim 1. Baschirotto, Fletcher, Saito and Varadarajan did not disclose various details of the clock generator and the phase-variance device.

42. Larson discloses a circuit configuration comprising a clock generator [square wave generator circuit 20] and a phase variance device [ring oscillator 40] embodied as an external squarewave generator [25] producing a squarewave signal [col.2, ll.50-51] and a divider circuit [primarily ring oscillator 40] connected to the squarewave generator, the divider circuit generating the at least two switching-clock signals from the squarewave signal [col.2, l.49 – col.3, l.39; lines 22 and 24 produce the two different phase signals with the output being controlled by terminal 56].

43. It would have been obvious to one of ordinary skill in the art, having the teachings of Larson, Baschirotto, Fletcher, Saito and Varadarajan before him at the time the invention was made, to use the clock generator and phase-variance device taught by Larson for the circuit configuration disclosed by Baschirotto, Fletcher, Saito and Varadarajan as the clock generator and phase-variance device taught by Larson is suitable for use in the circuit

configuration of Baschirotto, Fletcher, Saito and Varadarajan. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to reduce power consumption [finding 6.5].

44. As to claim 14, Baschirotto discloses the circuit configuration wherein the squarewave signal has a duty ratio [fig.5; inherently, squarewaves generated have an associated duty ratio with the ideal being 1:1]. Fletcher discloses adjustment of the duty ratio varies the switching-clock phases in which the first and second switching-clock signals are in the off-phase [col.8, ll.41-65; col.17, l.33 – col.19, l.11; col.20, l.50 – col.21, l.18].

45. Claims 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baschirotto and Fletcher, as applied to claims 17 and 21 above, and further in view of Saito.

46. Baschirotto and Fletcher disclose each and every limitation of the claim as discussed above in reference to claims 17 and 21 above. Baschirotto did not discuss a detector for detecting the switching speed of the transistors. Saito discloses a circuit configuration, comprising a detector for detecting the switching speed of the transistors [finding 7.1] in order to optimize processing [finding 7.2]. It would have been obvious to one of ordinary skill in the art, having the teachings of Baschirotto, Fletcher and Saito before him at the time the invention was made, to use the detector taught by Saito for the circuit configuration disclosed by Baschirotto and Fletcher as the detector taught by Saito is suitable for use in the circuit configuration of Baschirotto and Fletcher. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to optimize processing.

47. Claims 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baschirotto and Fletcher as applied to claim 17 above, and further in view of Larson.

48. In re claim 25, Baschirotto and Fletcher disclose each and every limitation of the claim, as discussed above in reference to claim 17. Baschirotto did not disclose the details of a specific clock generator for generating the clock signals.

49. Larson discloses a method for generating clock signals [frequency] [col.1, ll.8-10] with a programmable clock generator [frequency divider 10] [col.2, l.67 – col.3, ll.39; clock generator is programmed through terminal 56 to output appropriate clock signals].

50. It would have been obvious to one of ordinary skill in the art, having the teachings of Larson, Fletcher and Baschirotto before him at the time the invention was made, to use the programmable clock generator taught by Larson in the method disclosed by Baschirotto and Fletcher as the clock generator taught by Larson is suitable for use in the method of Baschirotto and Fletcher to produce the at least two non-overlapping switching-clock signals. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to produce the switching-clock signals.

51. As to claim 26, see discussion above in reference to claim 25. Larson discloses a method for generating clock signals with an external squarewave generator [25] and a divider circuit [primarily ring oscillator 40].

52. As to claim 27, Fletcher discloses the method comprising varying the switching-clock phases in which the operational amplifiers are switched off by adjusting a duty ratio of a s signal from the generator [col.8, ll.41-65; col.17, l.33 – col.19, l.11; col.20, l.50 – col.21, l.18].

53. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Baschirotto and Fletcher as applied to claim 17 above, and further in view of Inoshita as applied to claim 7 above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (571) 272-3672. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tse Chen
October 6, 2005

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100